

AMC *to* SMA Ultra 9000



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Revision History

Rev	Date	Comments
0.9	Jan 1, 2012	Initial Release
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Support:

Additional support information may be found at www.silicontkx.com

Warranty:

To assure all future engineering notifications are communicated the enclosed warranty information must be completed.

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The following information is intended to alert the user to possible dangers and important information contained within this guide. The “**WARNINGS**” and “**NOTES**” do not eliminate these dangers. Close attention to the information supplied along with “common sense” operation is the major accident prevention measure.

WARNING:	Failure to follow this warning may result in bodily injury.
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NOTE:	Failure to follow this note may result in improper results from the board.
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Reference Websites

Below is a list of websites that can be used to obtain additional information and details that may not be fully provided in this manual.

Advanced Mezzanine Card www.picmg.org
RapidIO..... www.rapidio.org

Manual Definitions

There are several important definitions or abbreviations use throughout this manual.

SubMiniature version A connector is referred to by the common abbreviation **SMA**.

Advanced Mezzanine Card is referred to by the common abbreviation **AMC**.

The ‘AMC to SMA Ultra 9000’ is referred to as **Ultra 9000**.

See Glossary at the end of this manual for a complete set of terms and abbreviations.

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List of Included Accessories

- User Manual (on CD)
- Schematic (on CD)

1.0 General Description

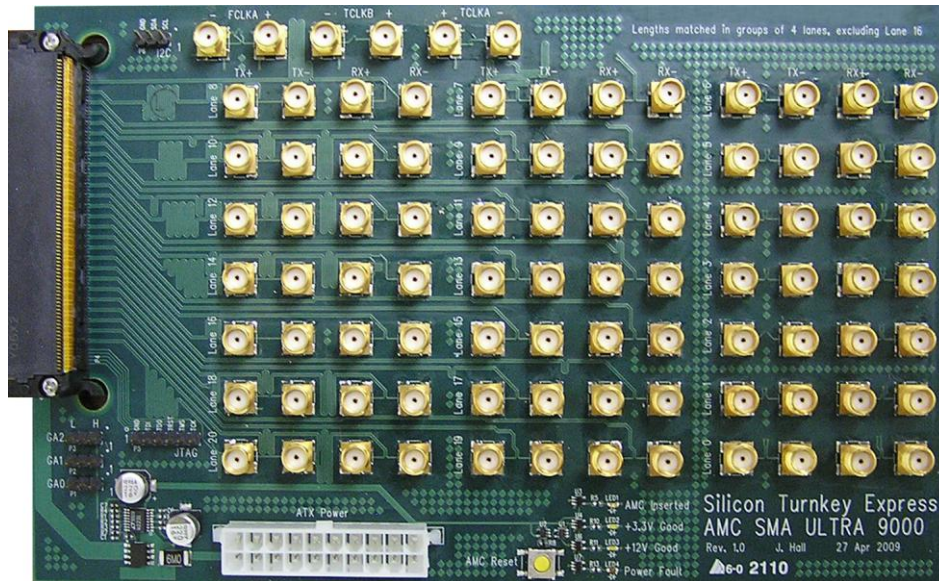


Figure 1 – Ultra 9000

The AMC to SMA Ultra 9000 is a single AMC Carrier platform for development engineering to connect SMAs to every serdes signal on an AMC module. The Ultra 9000 includes 42 differential parts of signals, 21 transmit and 21 receive. It can be used for AMC.1 1000BASE –BX signals, AMC.3 STAT/SAS signals, AMC.4 Serial RapidIO Ports (FAT PIPE: AMC.1 x 4 PCIe; AMC.4 x S-RIO; AMC.2 10GB Base – BX4), as well as Extended FAT PIPE (disputed Ports between AMC.4 S-RIO and AMC.2 1-0G Base – BX4), and Extended Options Scope Ports per V 1.0. The carrier is powered with a standard ATX power supply. Besides providing power to the AMC socket it allows direct control to the AMC reset and Geographical Addresses, and provides connections for I2C and JTAG and synchronization clock signals.

The Ultra 9000 can be manufactured with all SMAs or partial depopulated to fit the designers needs. Contact Silicon Turnkey Express for further details.

1.1 Device Placement and Functions

This section provides a description of the connectors, jumpers, switches and main components of the board. Refer to Figure 2 for location of the devices referenced below.

Additional descriptions of the switches and jumpers with their recommended settings will be in Section 3.

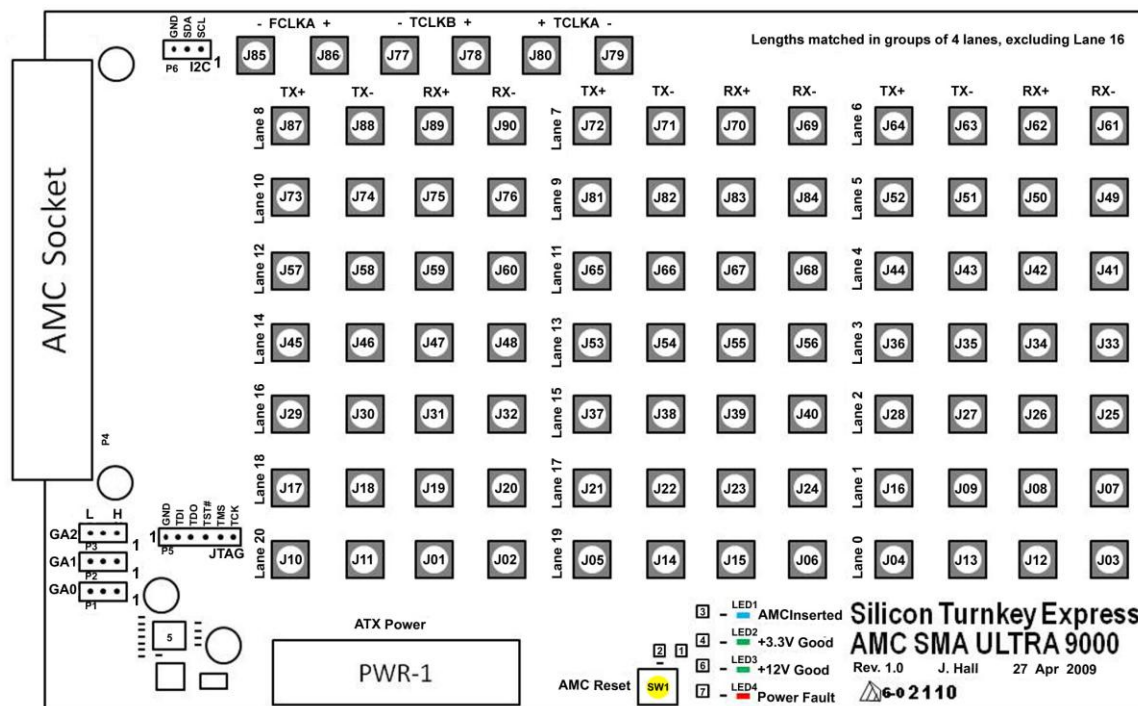


Figure 2 –Top Board Layout

1.1.1 J01 – J90

Lighthouse, LTI, 26.5GHz. SMA connectors from all port signals. See Section 3.1 for connector assignments.

1.1.2 LED1 (Blue)

Indicates when an AMC card is recognized in socket P4.

1.1.3 LED2 (Green)

Indicates +3.3V is good.

1.1.4 LED3 (Green)

Indicates +12V is good.

1.1.5 LED4 (Red)

Indicates power fault.

1.1.6 P01 – P03

Geographic Addresses

Single 3 pin 0.1" header. See Section 3.2 for more details.

1.1.17 P04 – AMC Socket

Yamaichi CN074 AMC.
See Appendix A for pin out.

1.1.18 P05 – JTAG Connector

Single 6 pin 0.1" header.
Directly connected to Yamaichi connector.

1.1.19 P06 – I²C Header

Single 3 pin 0.1" header.
Directly connected to Yamaichi connector.

1.1.20 SW1 – AMC Reset

Momentary switch creates an input to AMC_EN on the AMC connector when +3.3V and +12V are present and switch is actuated.

2.0 Hardware Design & Architecture

2.1 General Description

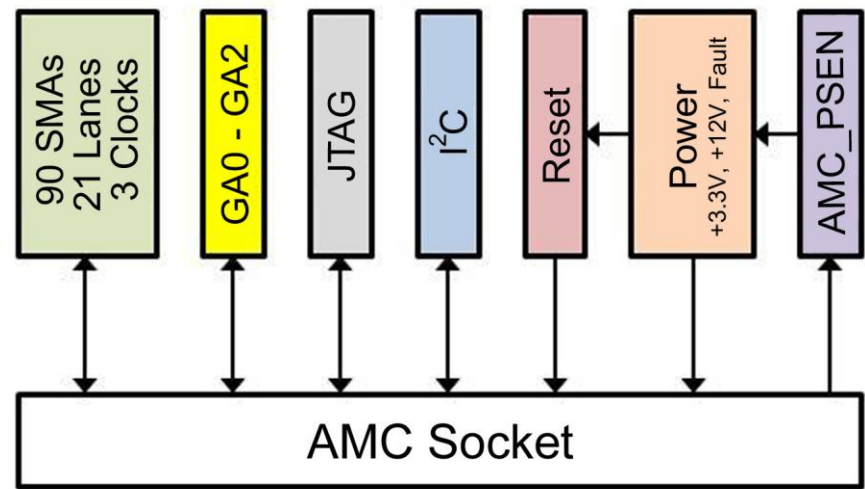


Figure 3- Block Diagram of Board

2.2 Physical Specifications

This section contains general information on the physical characteristics.

Board Size	127mm x 203mm
Power Requirement (to support an AMC)	ATX Power Supply, 100W
Operating Temperature	
Standard Version	0 ⁰ to +70 ⁰ C
Industrial Version	-40 ⁰ to +85 ⁰ C
Weight.....	240g

3.0 Design Theory and Settings

This section contains information on the Ultra 9000 design and layout. It provides details of jumpers and setting available. More information on Advanced Mezzanine Card design theory is available at www.picmg.org. Information on RapidIO is available at www.com.

3.1 Transmit and Receive Lanes

A Lane is a set of differential signal pairs, one pair for transmission and one pair for reception. One or more Lanes operate together to form a Link. E-keying definition of a differential pair is associated with a specific Fabric Link, Lanes [x:0].

In the Ultra 9000 all Lanes from the AMC socket to SMA connectors are matched for impedance except Lane 16. Each differential pair of Lane 16's (transmit and receive) are impedance matched. Lane 16 as defined in R1.0 of the AMC.0 specification has been re-defined for use as TCLKC and TCLKD. See Appendix A for Lane definition and AMC socket to Ultra 9000 SMA mapping.

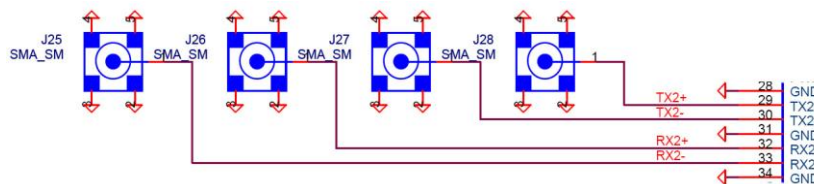


Figure 4 – Lane Pair Example

3.2 Geographic Address

Three Geographic Address (GA) pins are used to assign the address of a Module on Intelligent Platform Management Interface, IPMI. Each of the GA pins can encode three different levels; they can be connected to Logic Ground, to Management Power, or left unconnected on the Carrier to define the Geographic Address of the Module. See the AMC specifications for additional information.

The Ultra 9000 connects the AMC Socket GA0, GA1 and GA2 directly to headers' pin 2 of P1, P2 and P3 respectively. Pin 1 of the header is +3.3 Volts and pin 3 is ground.

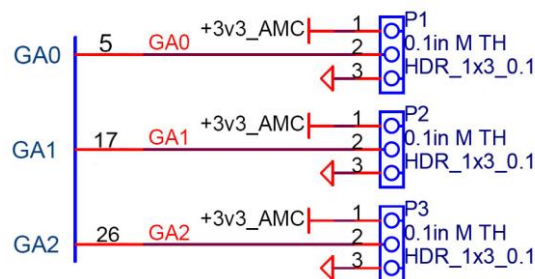


Figure 5 – Geographic Address Headers

3.2 JTAG

This provides an industry standard method of performing manufacturing test and verification and is critical to the test of today's complex products that are often making extensive use of BGA device packages. The Ultra 9000 JTAG header is connected directly to AMC connector.

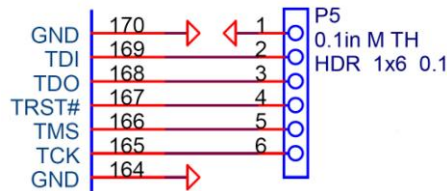


Figure 6 – JTAG Circuit

3.3 I²C

IPMB is a bus made up of clock (SCL_L) and data (SDA_L) I²C signals. The Ultra 9000 provide a header for this signals that are connected directly to the AMC connector.

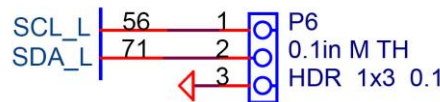


Figure 7 – I2C Circuit

3.4 Reset

The ENABLE# pin on the AMC connector is an active low input to the Module pulled up on the Module to Management Power (MP). This signal is inverted on the Module to create an MMC RESET# signal. This input indicates to the Module that the Module is fully inserted and valid states exist on all inputs to the Module. The MMC is not allowed to read the GA inputs or use the IPMB while ENABLE# is inactive.

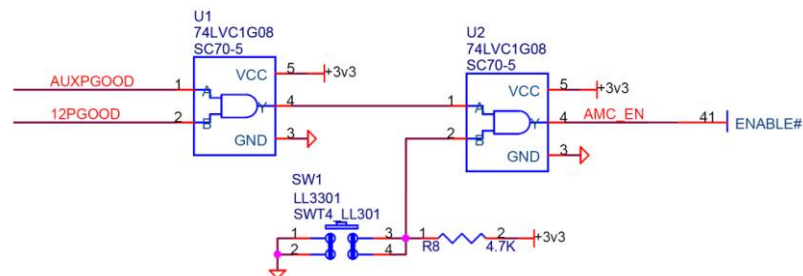


Figure 8 – Reset Circuit

3.5 Power Supply

A standard ATX power supply provides +3.3V and +12V to a Dual Supply Hot Swap Controller, U5. The controller generates voltages to the AMC socket as well as senses the AMC and provides fault information to the Ultra 9000.

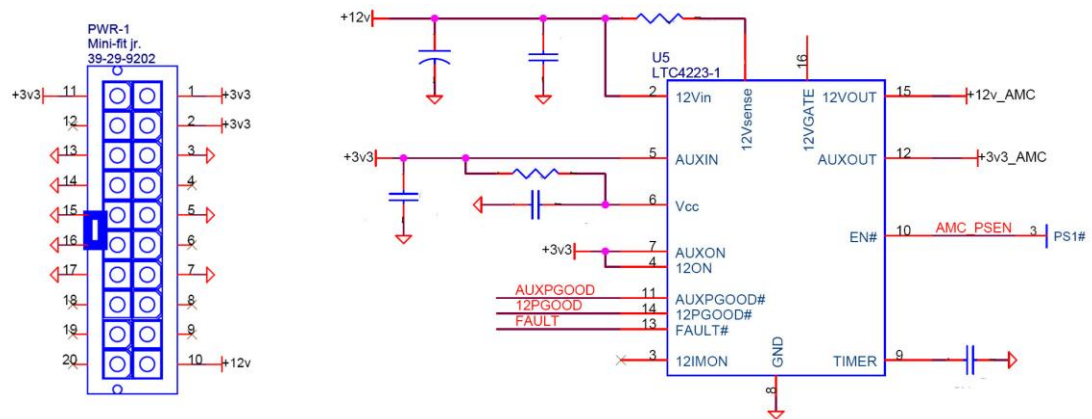


Figure 9 – Power Sense Circuit

3.6 LED Indicators

The Ultra 9000 four LEDs provide information from the power supply controller for AMC Insertion (Blue), +3.3V and +12V Good (Green), and AMC power supply Fault condition (Red).

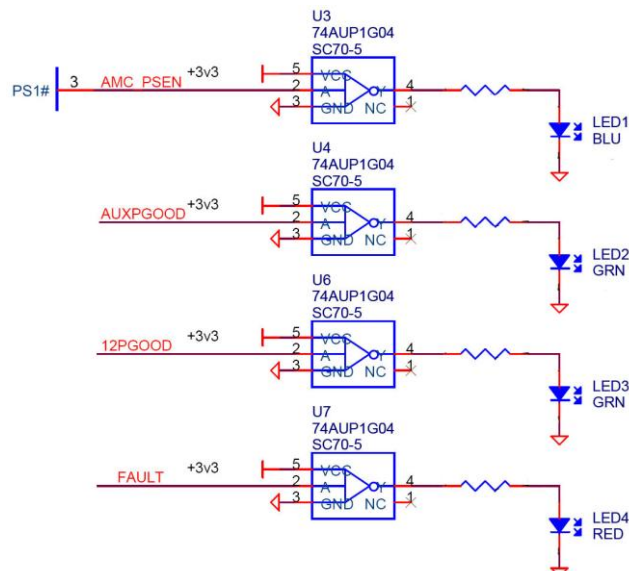


Figure 10 - LEDs

3.7 Synchronization Clock Interface

The Synchronization Clock Interface provides three differential pairs for clock distribution to enable applications that require the exchange of synchronous timing information among Modules and consequently multiple boards in a Shelf. This allows Modules to source clock(s) to the system in the case where it provides a Network Interface function, or conversely to receive timing information from another Carrier Board or Module within the system. The three Synchronization Clock signals are TCLKA, TCLKB, and FCLKA, each supported by a differential pair.

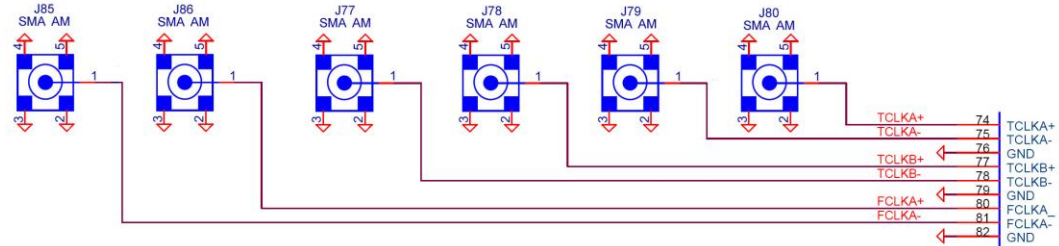


Figure 11 – Synchronization Clocks

Appendix A – AMC Socket to Ultra 9000 Map

The following AMC Socket pin out maps the AMC to SMA Ultra 9000 and STx's AMC to SMA Ultra 15000 series (standard 1U). The definitions shown are as of April 2009.

AMC.2 1000BASE-BX						
AMC.3 SATA/SAS						
AMC.4 S-RIO Ports (FAT PIPE; AMC.1 x 4 PCIe; AMC.4 x4 SRIO; AMC.2 10G Base-BX4)						
Extended Fat Pipe; Disputed Ports Between AMC.4 SRIO and AMC.2 10G Base-BX4						
Extended Options Scope Ports per V 1.0						
Pin	Definition	Function	Ultra 9K Connection	Insertion Sequence	Present in Ultra 15K	
					Extended	Basic +
1	GND	GND		First		
2	PWR	+12V_AMC		First		
3	PS1#	AMC_PSEN	U5 - 10	Last	YES	YES
4	MP	+3v3_AMC		Second		
5	GA0	GA0	P1 - 2	Second	YES	YES
6	RSVD6	NC		Second		
7	GND	GND		First		
8	RSVD8	NC		Second		
9	PWR	+12V_AMC		First		
10	GND	GND		First		
11	TX0+	TX0+	J04 -1	Third	YES	YES
12	TX0-	TX0-	J13 -1	Third	YES	YES
13	GND	GND		First		
14	RX0+	RX0+	J12 -1	Third	YES	YES
15	RX0-	RX0-	J03 -1	Third	YES	YES
16	GND	GND		First		
17	GA1	GA1	P2 - 2	Second		
18	PWR	+12V_AMC		First		
19	GND	GND		First		
20	TX1+	TX1+	J16 - 1	Third	YES	YES
21	TX1-	TX1-	J09 - 1	Third	YES	YES
22	GND	GND		First		
23	RX1+	RX1+	J08 - 1	Third	YES	YES
24	RX1-	RX1-	J07 -1	Third	YES	YES
25	GND	GND		First		
26	GA2	GA2	P3 - 2	Second	YES	YES
27	PWR	+12V_AMC		First		

AMC Socket to Ultra 9000 Map continued

Pin	Definition	Function	Ultra 9K Connection	Insertion Sequence	Present in Ultra 15K	
					Extended	Basic +
28	GND	GND		First		
29	TX2+	TX2+	J28 - 1	Third	YES	YES
30	TX2-	TX2-	J27 - 1	Third	YES	YES
31	GND	GND		First		
32	RX2+	RX2+	J26 -1	Third	YES	YES
33	RX2-	RX2-	J25 -1	Third	YES	YES
34	GND	GND		First		
35	TX3+	TX3+	J36 - 1	Third	YES	YES
36	TX3-	TX3-	J35 - 1	Third	YES	YES
37	GND	GND		First		
38	RX3+	RX3+	J34 - 1	Third	YES	YES
39	RX3-	RX3-	J33 - 1	Third	YES	YES
40	GND	GND		First		
41	ENABLE#	AMC_EN	U2 - 4	Second	YES	YES
42	PWR	+12V_AMC		First		
43	GND	GND		First		
44	TX4+	TX4+	J44 -1	Third		YES
45	TX4-	TX4-	J43 -1	Third		YES
46	GND	GND		First		
47	RX4+	RX4+	J42 -1	Third		YES
48	RX4-	RX4-	J41 -1	Third		YES
49	GND	GND		First		
50	TX5+	TX5+	J52 -1	Third		YES
51	TX5-	TX5-	J51 -1	Third		YES
52	GND	GND		First		
53	RX5+	RX5+	J50 -1	Third		YES
54	RX5-	RX5-	J49 -1	Third		YES
55	GND	GND		First		
56	SCL_L	SCL	P6 - 1	Second	YES	YES
57	PWR	+12V_AMC		First		
58	GND	GND		First		
59	TX6+	TX6+	J64 -1	Third		YES
60	TX6-	TX6-	J63 -1	Third		YES
61	GND	GND		First		
62	RX6+	RX6+	J62 -1	Third		YES
63	RX6-	RX6-	J61 -1	Third		YES
64	GND	GND		First		

AMC Socket to Ultra 9000 Map continued

Pin	Definition	Function	Ultra 9K Connection	Insertion Sequence	Present in Ultra 15K	
					Extended	Basic +
65	TX7+	TX7+	J72 -1	Third		YES
66	TX7-	TX7-	J71 -1	Third		YES
67	GND	GND		First		
68	RX7+	RX7+	J70 -1	Third		YES
69	RX7-	RX7-	J69 -1	Third		YES
70	GND	GND		First		
71	SDA_L	SDA	P6 - 2	Second	YES	YES
72	PWR	+12V_AMC		First		
73	GND	GND		First		
74	TCLKA+	TCLKA+	J80 -1	Third	YES	YES
75	TCLKA-	TCLKA-	J79 - 1	Third	YES	YES
76	GND	GND		First		
77	TCLKB+	TCLKB+	J78 - 1	Third	YES	YES
78	TCLKB-	TCLKB-	J77 - 1	Third	YES	YES
79	GND	GND		First		
80	FCLKA+	FCLKA+	J86 - 1	Third	YES	YES
81	FCLKA-	FCLKA-	J85 -1	Third	YES	YES
82	GND	GND		First		
83	PS0#	GND		Last		
84	PWR	+12V_AMC		First		
85	GND	GND		First		
86	GND	GND		First		
87	RX8-	RX8-	J90	Third		YES
88	RX8+	RX8+	J89	Third		YES
89	GND	GND		First		
90	TX8-	TX8-	J88	Third		YES
91	TX8+	TX8+	J87	Third		YES
92	GND	GND		First		
93	RX9-	RX9-	J84	Third		YES
94	RX9+	RX9+	J83	Third		YES
95	GND	GND		First		
96	TX9-	TX9-	J82	Third		YES
97	TX9+	TX9+	J81	Third		YES
98	GND	GND		First		
99	RX10-	RX10-	J76	Third		YES
100	RX10+	RX10+	J75	Third		YES
101	GND	GND		First		

AMC Socket to Ultra 9000 Map continued

Pin	Definition	Function	Ultra 9K Connection	Insertion Sequence	Present in Ultra 15K	
					Extended	Basic +
102	TX10-	TX10-	J74	Third		YES
103	TX10+	TX10+	J73	Third		YES
104	GND	GND		First		
105	RX11-	RX11-	J68	Third		YES
106	RX11+	RX11+	J67	Third		YES
107	GND	GND		First		
108	TX11-	TX11-	J66	Third		YES
109	TX11+	TX11+	J65	Third		YES
110	GND	GND		First		
111	RX12-	RX12-	J60	Third	YES	
112	RX12+	RX12+	J59	Third	YES	
113	GND	GND		First		
114	TX12-	TX12-	J58	Third	YES	
115	TX12+	TX12+	J57	Third	YES	
116	GND	GND		First		
117	RX13-	RX13-	J56	Third	YES	
118	RX13+	RX13+	J55	Third	YES	
119	GND	GND		First		
120	TX13-	TX13-	J54	Third	YES	
121	TX13+	TX13+	J53	Third	YES	
122	GND	GND		First		
123	RX14-	RX14-	J48	Third	YES	
124	RX14+	RX14+	J47	Third	YES	
125	GND	GND		First		
126	TX14-	TX14-	J46	Third	YES	
127	TX14+	TX14+	J45	Third	YES	
128	GND	GND		First		
129	RX15-	RX15-	J40	Third	YES	
130	RX15+	RX15+	J39	Third	YES	
131	GND	GND		First		
132	TX15-	TX15-	J38	Third	YES	
133	TX15+	TX15+	J37	Third	YES	
134	GND	GND		First		
135	RX16-	RX16-	J32	Third	YES	
136	RX16+	RX16+	J31	Third	YES	
137	GND	GND		First		
138	TX16-	TX16-	J30	Port	YES	

AMC Socket to Ultra 9000 Map continued

Pin	Definition	Function	Ultra 9K Connection	Insertion Sequence	Present in Ultra 15K	
					Extended	Basic +
139	TX16+	TX16+	J29	Third	YES	
140	GND	GND		First		
141	RX17-	RX17-	J24	Port	YES	
142	RX17+	RX17+	J23	Third	YES	
143	GND	GND		First		
144	TX17-	TX17-	J22	Third	YES	
145	TX17+	TX17+	J21	Third	YES	
146	GND	GND		First		
147	RX18-	RX18-	J20	Third	YES	
148	RX18+	RX18+	J19	Third	YES	
149	GND	GND		First		
150	TX18-	TX18-	J18	Third	YES	
151	TX18+	TX18+	J17	Third	YES	
152	GND	GND		First		
153	RX19-	RX19-	J06	Third	YES	
154	RX19+	RX19+	J15	Third	YES	
155	GND	GND		First		
156	TX19-	TX19-	J14	Third	YES	
157	TX19+	TX19+	J05	Third	YES	
158	GND	GND		First		
159	RX20-	RX20-	J02	Third	YES	
160	RX20+	RX20+	J01	Third	YES	
161	GND	GND		First		
162	TX20-	TX20-	J11	Third	YES	
163	TX20+	TX20+	J10	Third	YES	
164	GND	GND		First		
165	TCK	TCK	P5 - 6	Second	YES	YES
166	TMS	TMS	P5 - 5	Second	YES	YES
167	TRST#	TRST#	P5 - 4	Second	YES	YES
168	TDO	TDO	P5 - 3	Second	YES	YES
169	TDI	TDI	P5 - 2	Second	YES	YES
170	GND	GND		First		
M1 to M8	M1 to M8					

Appendix B – Connector Pin Assignments

J01 to J90 – SMA

Lighthouse, LTI, 26.5 GHz, Vertical
See Appendix A for pin connection

P01– Geographic Address GA0

3 pin header 0.1

Pin No	Description
1	+3.3V
2	GA0
3	GND

P02– Geographic Address GA1

3 pin header 0.1

Pin No	Description
1	+3.3V
2	GA1
3	GND

P03– Geographic Address GA2

3 pin header 0.1

Pin No	Description
1	+3.3V
2	GA2
3	GND

P04 – AMC Socket

Yamaichi
See Appendix A for pin out

P05– JTAG

6 pin header 0.1

Pin No	Description
1	GND
2	TDI
3	TDO
4	TST#
5	TMS
6	TCK

P06– I2C (IPMB)

3 pin header 0.1

Pin No	Description
1	SCL
2	SDA
3	GND

PWR-1– Power Input (ATX)

Molex 39-01-2200

Pin No	Description
1	+3.3V
2	+3.3V
3	GND
4	NC
5	GND
6	NC
7	GND
8	NC
9	NC
10	+12v
11	+3.3v
12	NC
13	GND
14	GND
15	GND
16	GND
17	GND
18	NC
19	NC
20	NC

Glossary

Here is a list of terms, acronyms and definitions that may be incorporated in this manual.

Acronyms

AMC	Advanced Mezzanine Card
ATAC	Advanced Telecommunications Computing Architecture
ATX	Advanced Technology Extended (mother board form factor)
CPLD	Complex Programmable Logic Device
CPU	Central Processor Unit
DMA	Direct Memory Access
DSP	Digital Signal Processor
FRU	Field Replaceable Units
GA	Geographic Address
GIGE	Gigabit Ethernet
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Test Port per IEEE 1149
MMC	Module Management Controller
MP	Management Power
OOB	Out of Band
PCIe	Peripheral Component Interconnect Express
PICMG	PCI Industrial Computer Manufacturers Group
PMC	PCI Mezzanine Card
RAM	Random Access Memory
SCL	Serial Clock (use with I2C Bus or IPMB)
SDA	Serial Data (use with I2C Bus or IPMB)
S-RIO (SRIO)	Serial RapidIO
TCK	Test Clock (use with JTAG)
TDI	Test Data In (use with JTAG)
TDO	Test Data Out (use with JTAG)
TMS	Test Mode Select (use with JTAG)
TST# (TRST)	Test Reset Input (use with JTAG)

Definitions

AMC.x	AdvancedMC is targeted to requirements for the next generation of "carrier grade" communications equipment. This series of specifications are designed to work on any carrier card and controlled by over 100 companies known as the PCI Industrial Computers Manufactures Group, PICMG.
Fat Pipe	A Fat Pipe is a data transmission circuit or network that is capable of carrying large amounts of data without significantly degrading the speed of transmission.
Lane	A set of differential signal pairs, one pair for transmission and one pair for reception. One or more Lanes operate together to form a Link.
Link	A group of Lanes which operate together to connect two devices; the number of Lanes used is negotiated.
Port	A set of differential signal pairs, one pair for transmission and one pair for reception.
SerDes	(serializers/deserializers) are devices that can take wide bit-width, single-ended signal buses and compress them to a few, typically one, differential signal that switches at a much higher frequency rate than the wide single-ended data bus.
Shelf	The Shelf consists of the Subrack, Backplane, Front Boards, cooling deices, RTMs, power suppliers, etc. Also historically known as a chassis.